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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/683,932	SCHULZ ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,11-14,28 and 32-34* is/are allowed.

6)☒ Claim(s) *1-3, 5-10, 15-27, 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/19/05,11/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-10, 15-22 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Galicki et al., US Patent 6,982976, herein referred to as Galicki. Referring to claim 1, Galicki has taught a pipeline accelerator, comprising:

a. a communication bus (column 6, lines 18-25, The processors are connected by a communication bus.);

b. a plurality of clock signal lines operable to carry at least a first clock signal and a second clock signal, the first and second clock signals being unsynchronized with one another (column 6, lines 18-25, The processors have unsynchronized clock sources.); and

c. a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit, including a first hardwired-pipeline circuit that is coupled to receive and is operable synchronously with the first clock signal and at least one other hardwired-pipeline circuit that is coupled to receive and is operable synchronously with the second

clock signal (column 6, lines 18-25, The two processors are the hardwired pipeline circuits. The processors have unsynchronized clock sources.).

3. Referring to claim 2, Galicki has taught the pipeline accelerator of claim 1, as described above, and wherein each of the pipeline units comprises:

a. a respective memory coupled to the hardwired-pipeline circuit (Internal I/O RAM, Figures 1, 3, 4, 7, 8, 9, Figure 23 SYNC FIFO); and

b. wherein the hardwired-pipeline circuit is operable to, receive data from the communication bus, load the data into the memory, retrieve the data from the memory, process the retrieved data, and drive the processed data onto the communication bus (Figures 1, 3, 4, 7, 8, 9, Data received by the processor is loaded into the I/O RAM, processed, results stored back in I/O RAM and then transmitted to the communication bus, see column 3, lines 42-45).

4. Referring to claim 3, Galicki has taught the pipeline accelerator of claim 1, as dedscribed above, and wherein each of the pipeline units comprises:
a respective memory coupled to the hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, I/O RAM); and wherein the hardwired-pipeline circuit is operable to, receive data from the communication bus (column 3, lines 50-55), process the data (Figure 4, element 400, at least the CPU core processes the data, see column 4, line 54-column 5, line 8), load the processed data into the memory (Figures 1, 3, 4, 7, 8, 9, I/O RAM), retrieve the processed data from the memory, and load the retrieved data onto the communication

bus (Figures 1, 3, 4, 7, 8, 9, Data is transmitted from the I/O RAM onto the communication bus between the processors).

5. Referring to claim 5, Galicki has taught the pipeline accelerator of claim 1, as described above, and further comprising:

a. a pipeline bus (Figure 4, Bus from I/O RAM to the DMA); and

b. a pipeline-bus interface coupled to the communication bus and to the pipeline bus (Figure 4, I/O RAM is the interface for the two busses).

6. Referring to claim 6, Galicki has taught the pipeline accelerator of claim 1, as described above, and further comprising:

a. wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit (Figure 25); and

b. a router coupled to each of the branches (Figure 25, column 19, lines 3-41).

7. Referring to claim 7, Galicki has taught the pipeline accelerator of claim 1, as described above, and further comprising:

a. wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit (Figure 25);

b. a router coupled to each of the branches (Figure 25, column 19, lines 3-41);

c. a pipeline bus (Figure 4, Bus from I/O RAM to the DMA); and

a pipeline-bus interface coupled to the router and to the pipeline bus (Figure 4, I/O RAM is the interface for the two busses).

8. Referring to claim 8, Galicki has taught the pipeline accelerator of claim 1, as described above, and further comprising:

a. wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit (Figure 25);

b. a router coupled to each of the branches (Figure 25, column 19, lines 3-41);

c. a pipeline bus (Figure 4, Bus from I/O RAM to the DMA);

d. a pipeline-bus interface coupled to the router and to the pipeline bus (Figure 4, I/O RAM is the interface for the two busses); and

e. a secondary bus coupled to the router (Figure 25, column 19, lines 3-41, several bidirectional busses are coupled to the routers.).

9. Referring to claim 9, Galicki has taught the pipeline accelerator of claim 1, as described above, and wherein:

a. the communication bus is operable to receive data addressed to one of the pipeline units (column 6, lines 18-25, Figures 1, 3, 4, 7, 8, 9, 23 and 25, Data

is transmitted and received to and from each processor through a communication bus.); and

b. the one pipeline circuit is operable to accept the data (A data packet is transmitted for a particular processor. Figure 5, Column 6, lines 3-17); and

c: the other pipeline circuits are operable to reject the data (Figure 5, Column 6, lines 3-17, Packet is routed back out.).

10. Referring to claim 10, Galicki has taught the pipeline accelerator of claim 1, as described above, and further comprising:

a. wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit (Figure 25);

b. a router coupled to each of the branches and operable to,
receive data addressed to one of the pipeline units (Figure 25), and

c. provide the data to the one pipeline unit via the respective branch of the communication bus (Figure 25, Figure 25, column 19, lines 3-41).

11. Referring to claim 30, Galicki has taught the pipeline accelerator of claim 1, as described above, and wherein at least one of the respective hardwired-pipeline circuits is disposed on an application-specific
integrated circuit (Figure 4).

12. Referring to claim 15, Galicki has taught a method, comprising:

a. sending via a communication bus first data and second data to first and second ones, respectively, of a plurality of pipeline units, each pipeline unit including a respective hardwired pipeline (column 6, lines 18-25);

b. processing the first data with the first pipeline unit synchronized to a first clock signal (column 6, lines 18-25, The processors are unsynchronized.); and

c. processing the second data with the second pipeline unit-synchronized to a second clock signal and while the first pipeline unit is processing the first data, the second clock signal being unsynchronized to the first clock signal (column 6, lines 18-25, The processors are operating in parallel in an unsynchronized manner.).

13. Referring to claim 16, Galicki has taught the method of claim 15, as described above, and wherein sending the data comprises:

a. sending the data to a router (Figure 25, column 19, lines 3-41); and

b. providing the first data to the first pipeline unit with the router via a respective first branch of the communication bus (Figure 25, column 19, lines 3-41).

14. Referring to claim 17, Galicki has taught the method of claim 15, as described above, and wherein sending the first data comprises sending the first data to the first

pipeline unit with a processor (Figure 25, column 19, lines 3-41, column 6, lines 18-25, The processors send and receive data to and from one another.).

15. Referring to claim 18, Galicki has taught the method of claim 15, as described above, and wherein sending the first data comprises sending the first data to the first pipeline with a third of the plurality of pipeline units (column 6, lines 18-25, All of the processors send and receive data to and from one another.).

16. Referring to claim 19, Galicki has taught the method of claim 15, as described above, and further comprising driving the processed first data onto the communication bus with the first pipeline unit (column 6, lines 18-25, The processor send and receive data to and from one another. Data from the processors is driven on the bus by I/O RAM, see Figures 1, 3, 4, 7, 8, 9)

17. Referring to claim 20, Galicki has taught the method of claim 15, as described above, and wherein processing the first data with the first pipeline unit comprises:

a. receiving the first data from the communication bus with a hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, Figure 25, column 19, lines 3-41, column 6, lines 18-25, The processors receive data.),

b. loading the first data into a memory with the hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, I/O RAM), retrieving the first data from the memory with the hardwired-pipeline circuit, and processing the retrieved first data with the hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, Data received by the processor

is loaded into the I/O RAM, processed, results stored back in I/O RAM and then transmitted to the communication bus, see column 3, lines 42-45).

18. Referring to claim 21, Galicki has taught the method of claim 15, as described above, and further comprising:

a. wherein processing the first data with the first pipeline unit comprises, receiving the first data from the communication bus with a hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, Figure 25, column 19, lines 3-41, column 6, lines 18-25, The processors receive data.),

b. processing the received first data with the hardwired-pipeline circuit (column 19, lines 3-41, column 6, lines 18-25, The processors process the data.), and

c. loading the processed first data into a memory with the hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, I/O RAM); and

d. retrieving the processed first data from the memory and driving the processed first data onto the communication bus with the hardwired-pipeline circuit (Figures 1, 3, 4, 7, 8, 9, Data received by the processor is loaded into the I/O RAM, processed, results stored back in I/O RAM and then transmitted to the communication bus, see column 3, lines 42-45).

19. Referring to claim 22, Galicki has taught the method of claim 15, as described above, and further comprising:

a. generating a message that includes the first data and that identifies the first pipeline unit as a recipient of the message (A data packet is transmitted for a particular processor. Figure 5, Column 6, lines 3-17); and

b. wherein sending the first data to the first pipeline unit comprises determining from the message that the first pipeline is a recipient of the message (Figure 5, Column 6, lines 3-17, The packet is either processed or routed back out.).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galicki et al., US Patent 6,982976, herein referred to as Galicki.

22. Referring to claim 29, Galicki has taught the pipeline accelerator of claim 1, as described above. Galicki has not taught wherein at least one of the respective hardwired-pipeline circuits is disposed on a field-programmable gate array. However, having the circuitry be programmable would have increased the overall flexibility of the system so that it may be used for various applications. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the pipeline accelerator of Galicki include at least one of the respective hardwired-pipeline

circuits disposed on a field-programmable gate array, for the desirable purpose of increasing the overall flexibility of the system.

23. Claim 31 has nothing over claims 29 and 30 and claim 31 is rejected for the same reasons as set forth in claims 29 and 30.

24. Claims 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Ebeling et al (U.S. Patent # 6,023,742), herein referred to as Ebeling.

25. As per **claim 23**, Wong discloses a computing machine, comprising: a memory operable to store program instructions (See figure 3, LSM array and SDRAM: Both are connected to buses that can fetch instructions and thus can store program instructions); a program-instruction bus coupled to memory (See figure 3: The bus instruction fetch buses are program-instruction buses); a pipeline bus that is separate from the program-instruction bus (See figure 3: Memory instruction fetch bus, a pipeline bus, is different from the normal instruction fetch bus); a processor (See figure 3, CPU 302) coupled to the program-instruction bus and to the pipeline bus (See figure 3: All buses lead to the processor); the pipeline accelerator comprising, a communication bus (See Fig. 6, element 609; Col. 5, lines 24-26); a pipeline-bus interface coupled to the communication bus and to the pipeline bus (See fig. 3, elements 319a,b; col. 4, lines 22-24); and a plurality of pipeline units each coupled to the communication bus (See fig. 3, element "Datapath Slice"; Col. 5, lines 30-34) and each comprising a respective hardwired-pipeline circuit (See fig. 6, elements "DPU"; Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping...")).

26. Wong does not teach a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

27. Ebeling does disclose a pipeline accelerator inoperable to communicate directly with the program-instruction bus (See figure 8: The data path and instruction converge at one point).

28. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Wong with Ebeling because both inventions deal with reconfigurable data paths with emphasis for flexibility (See abstracts of both patents) and thus if one or more features belonging to a similar invention were desirable, it would be obvious to combine those features into the invention.

29. As per **claim 24**, Wong discloses a method, comprising: retrieving with a processor program instructions from a memory via a program-instruction bus (See figure 3: Memory instruction fetch and SDRAM instruction fetch is possible); executing the instructions with the processors (See figure 3: Done inherently with processor); and transferring information between the processor and pipeline units of a pipeline accelerator via a pipeline bus that is separate from the program-instruction bus (See figure 3: More than one type of bus is present).

30. Wong does not teach a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

31. Ebeling does disclose a pipeline accelerator inoperable to communicate directly with the program-instruction bus (See figure 8: The data path and instruction converge at one point).

32. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Wong with Ebeling because both inventions deal with reconfigurable data paths with emphasis for flexibility (See abstracts of both patents) and thus if one or more features belonging to a similar invention were desirable, it would be obvious to combine those features into the invention.

33. As per **claim 25**, Wong discloses wherein the information comprises data (Information is inherently data); wherein transferring the information comprises sending the data from the processor to the pipeline units (See figure 16: ACM can receive data from ALU); and processing the data with the pipeline units (See figure 16: ACM is connected to ALU).

34. As per **claim 26**, Wong discloses wherein the information comprises data (Information is inherently data); wherein transferring the information comprises sending the data from the pipeline units to the processor (See figure 16: ACM can receive data from ALU); and processing the data with the processor (See figure 16: ACM is connected to ALU).

35. As per **claim 27**, Wong discloses wherein the information comprises addresses of the pipeline units (See column 7, line 63- column 8, line 2).

Response to Arguments

36. Applicant's arguments on pages 11-12 with respect to claims 1-3 and 5-10 are moot in view of the new grounds of rejection.

37. Applicant's arguments filed with respect to claims 23-27 have been fully considered but they are not persuasive.

38. On page 14, Applicant argues in essence:

> *"Referring to Ebeling's FIG. 8, the instruction signals/bus 16 is apparently operable to communicate directly with the configurable cells 26 via the control path 21. In particular, Ebeling discloses (at column 10, line 65 to column 11, line 55) that LUTs 220 receive instruction signals 16 and convert them into "dynamic control signals" 21. The dynamic control signals 21 are then "passed to the associated cell 26 as the data is pipelined down the data path 12." This appears to indicate that Ebeling's "pipeline accelerator" is operable to communicate directly with the program instruction bus. "*

However, the LUT's are what make the pipeline accelerator inoperable to communicate directly with the program-instruction bus. The LUT's perform a conversion in a central location on the data making the pipeline accelerator inoperable to directly communicate with the program instruction bus (column 10, line 65 to column 11, line 55). Therefore this argument is moot.

Allowable Subject Matter

39. Claims 4, 11-14, 28 and 32-34 are allowed.

Conclusion

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLM

/Tonia L. Meonske/
Tonia L. Meonske
September 25, 2007